Remarks

In view of the following discussion, the applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U. S. C § 102. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

A. 35 U. S. C. § 102

1. Claims 1, 7 and are not anticipated by Nagasawa et al.

Claims 1, 7 and 15 stand rejected under 35 U. S. C. § 102(e) as being anticipated by Nagasawa et al. (U. S. Patent 6,069,869 issued May 30, 2000). The applicants submit that claims 1, 7 and 15 are not anticipated by this reference.

Claim 1 is directed to an apparatus for reading or writing markings of an optical recording medium having data markings arranged along a track and header markings arranged laterally offset with respect to the center track (*see*, specification at page 1, lines 6-12). The apparatus includes a header identification unit, a header sequence detector for detecting a sequence of laterally offset header markings, a track crossing detector and an intermediate track detector for generating an intermediate track signal (*see*, specification at page 2, lines 13-31). The intermediate track detector is connected to outputs of the header identification unit, of the track crossing detector and of the header sequence detector (*see*, specification at page 12, lines 17-33). The output signal of the header sequence detector is the sequence detecting signal SDS, indicating whether the output signal of the adder has a rising or a falling zero crossing relative to the output signal of the subtractor (*see*, specification at

page 12, lines 17-21). A rising zero crossing indicates that the header markings are located firstly on the left and then on the right of the track center and a falling zero crossing indicates the opposite sequence (*see*, specification at page 12, lines 21-28).

Applicants submit that the connecting point detector 19 (CPD) of Nagasawa et al. does not anticipate the header identification unit (HUI) of claim 1. The header identification unit (HUI) generates a header identification signal (*see*, specification at page 3, lines 26-27) and outputs the header identification signal when a header area is present (*see*, specification at page 6, lines 29-31). The header identification unit (HUI) "evaluates ... whether or not the light beam is close enough to the track center", in which case "a header identification signal is output" (*see*, specification at page 9, lines 9-17). In the variant described with respect to Fig 3, the header identification unit "has the task of comparing the amplitude of the header signals with a predetermined threshold, and of passing on the information that this threshold has been exceeded as information 'header present'" (*see*, specification at page 10, lines 29-34).

The connecting point detector 19 (CPD) of Nagasawa et al., in contrast, "determines whether the header region being scanned is at a connecting point, and hence whether polarity reversal is to be effected" (*see*, Nagasawa et al. at column 12, lines 16-18). Thus, in Nagasawa et al. only refers to certain ones of the headers, namely to those in the region 4a of Fig 1B, as opposed to regions 4b, where polarity does not reverse. From the quoted descriptions in our application the header identification unit (HIU) of claim 1, unlike the connecting point detector 19 (CPD) in Nagasawa et al., responds to every header being scanned, regardless of whether or not the header is at a polarity reversal.

Applicants submit that the track crossing detector (TCD) of claim 1 is not anticipated by the tracking sensor (TS) 11 of Nagasawa et al. The track crossing detector (TCD) "outputs a pulse or a corresponding signal in or near the maxima and minima of the track error signal" (*see*, specification at page 4, lines 16-18). The track crossing detector (TDC) "outputs a track crossing signal TC" (*see*,

specification at page 6, lines 35-36). The track crossing detector (TCD) "has two comparators which compare the track error signal with an upper and a lower threshold value, respectively. The output signals of the comparators are fed to an OR gate, which outputs a track crossing signal " (*see*, specification at page 13, lines 1-6), it "has a phase shifter, whose output signal is fed to a comparator. The output signal of the latter is fed to an edge detector, whose output signal is the track crossing signal" (*see*, specification at page 17, line 36 to page 18, line 1). The track crossing detector (TCD) "has the task of finding the maximum values of the track error signal" (*see*, specification at page 24, lines 26-28). The track crossing detector (TCD) outputs a binary (bi-level) signal.

The tracking sensor (TS) of Nagasawa et al., in contrast, is a "split photodetector" (*see*, Nagasawa et al. at column 11, line 66) receiving light (*see*, Nagasawa et al. at column 11, lines 65-66). "Photo-currents output from the respective half portions" of the tracking sensor (TS) are converted "into voltage signals" (*see*, Nagasawa et al. at column 12, lines 4-6). In Nagasawa et al., the tracking sensor (TS) is an analog component producing an analog output signal. Thus, the track crossing detector (TCD) of claim 1 is not anticipated by the tracking sensor (TS) of Nagasawa et al.

Applicants submit that the intermediate track detector (ITD) of claim 1 is not anticipated by the adder 28 of Nagasawa et al. The intermediate track detector (ITD) "is connected to outputs of the header identification unit, of the track crossing detector, and of the header sequence detector, and generates an intermediate track signal" (*see*, specification at page 2, lines 16-19). The intermediate track detector (ITD) "forms an intermediate track signal MZC [and] furthermore outputs a control signal CS" (*see*, specification at page 6, line 39 to page 7, line 2). As intermediate track signal MZC, "the output signal Q of the D flip-flop 44" is used (*see*, specification at page 14, lines 12-13). The MZC "[corresponds] to the mirror signal in the scanning of conventional recording media" (*see*, specification at page 14, lines 17-19), it "reproduces the position of the light beam 3 with respect to the data track" (*see*, specification at page 15,

lines 1-3). Thus, the intermediate track signal is bi-level in nature, one of the levels indicating the presence of a land track, and the other indicating a groove track.

The adder 28 of Nagasawa et al. "adds the tracking error signal generated by the wobble pits to the original tracking error signal" (*see*, Nagasawa et al. at column 12, lines 42-43). Both these signals being analog, the result is, of course, also analog. Thus, the intermediate track signal (ITD) of claim 1 is not anticipated by the adder 28 of Nagasawa et al.

Applicants further submit that the adder 28 of Nagasawa et al. is not connected to outputs of the connecting point detector 19, the tracking sensor 11 and wobble pit detector 22. With blocks 21, 23, and 26 intervening between connecting point detector 19 and adder 28, with blocks 13, 16, 26 intervening between the tracking sensor 11 and adder 28, and with blocks 24, 25, and 27 intervening between wobble pit detector 22 and adder 28, adder 28 is at best connected to signals derived from the outputs of blocks 19/11/22.

Additionally, applicants submit that the connecting point detector 19 in Nagasawa et al. does not evaluate a summation signal 15 of the detector signals. With blocks 17 and 18 intervening between the summation signal 15 and the connecting point detector 19, and with "PLL data detect" and "Pattern matching" being known to be sophisticated operations of arbitrary complexity and output, the connecting point detector 19 is at best evaluating a signal derived from a summation signal 15 of the detector signals.

Claim 7 depends directly from claim 1. For the same reasons as stated above for claim 1, claim 7 is also patentable over Nagasawa et al.

Applicants submit that Nagasawa et al. does not anticipate "checking a signal 16 derived from detector elements 11 for the presence of signal components which indicate the lateral offset of the header markings" as recited in applicants claim 15. In Nagasawa, signal 16 runs through a sample/hold circuit (S/H) 23 and/or through two adders 26, 28, before being output as tracking error signal 28. Checking for the presence of signal components indicating header

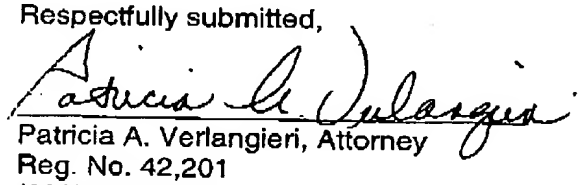
markings, i.e. wobble pit detection, is however performed in wobble pit detect 22, which receives as input a nameless signal coming from pattern matching 18. Thus, claim 15 is also patentable over Nagasawa et al.

CONCLUSION

Thus, the applicants submit that none of the claims, presently in the application are anticipated under the provisions of 35 U. S. C. § 102. Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867, so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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